PhD Thesis offer

Topic: Study and design of memory protections for an heterogeneous SoC architecture

Laboratory, team :

Laboratory Hubert Curien – UMR 5516 CNRS, University Jean Monnet Saint-Étienne Departament « *Informatique-Sécurité-Image »* – Team « *Systèmes Embarqués Sécurisés et Architectures Matérielles* »

Supervisors : Brice Colombier and Lilian Bossuet

Duration : 36 months

Start : 1st september or 1st october 2024

Location : Saint-Étienne, France

⮑ Description :

The *Systèmes Embarqués Sécurisés et Architectures Matérielles* (SESAM) team at the Hubert Curien Laboratory (UMR CNRS 5516 – Jean Monnet University) is one of the leading teams in cybersecurity for embedded systems at the national and international levels. Its main scientific activities revolve around three major areas that combine expertise in microelectronics and electronics, embedded systems, applied mathematics, and cryptography.

In the framework of the SCAMA project, funded by the *Agence Nationale de la Recherche* (ANR), the SESAM team is proposing a doctoral thesis. The objective of this thesis is to investigate potential architectural and micro-architectural attacks targeting the various memories of a heterogeneous SoC architecture (L1, L2, DDR) and to develop countermeasures that can be integrated into its hardware. The work aims to design effective and efficient memory protections, providing the flexibility to be activated or deactivated by a control element in the system based on the required security level. The targeted architecture will be multiprocessor, based on RISC-V cores, and will be implemented on an FPGA. It will include hardware accelerators, which can be reconfigurable or not, cryptographic and agile or not. Furthermore, this architecture will have the capability to collect and analyze the behavior of all its components through a security supervisor capable of detecting any intrusion or anomaly. For this last functionality, the use of machine learning algorithms will be necessary to ensure an efficient management of the platform.

⮑ Profile of the candidate :
- The candidate must have obtained a master degree in electronics, preferably in embedded systems, or have an equivalent degree.
- It is desirable that the candidate has knowledge in the design and implementation of architectures in FPGA (both AMD-Xilinx and Intel boards can be used during the thesis).
- The candidate must show capacity for communicating in english (verbal and written).
- Basic knowledge in the field of hardware or software security would be favorable.

⮑ How to apply :

The candidates must apply by sending their CV and a motivation letter by e-mail to Mr. Brice Colombier (b.colombier@univ-st-etienne.fr) and Mr. Lilian Bossuet (lilian.bossuet@univ-st-etienne.fr) as soon as possible.